REMARKS

Claims 1-19 are all of the claims presently pending in the application. Claims 1-4, 6-9, and 11-14 stand rejected on prior art grounds.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Regarding the prior art rejections, claims 1-19 stand rejected under 35 U.S.C. §103(a) as unpatentable over US Patent 5,742,842 to Suetake, further in view of US Patent 6,065,092 to Roy or US Patent 5,680,641 to Sidman.

This prior art rejections is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example, in independent claim 1, is directed to a computer system which includes a plurality of memory banks. A processor unit controls an overall processing of an operation. Additional processing units, each of which corresponds to one of the memory banks, performs a part of the operation independently of the processor unit. The operation is performed by the additional processing units, using data stored in the corresponding memory banks and based on an instruction or data provided from the processor unit. The plurality of memory banks are external to the processing unit and additional processing units.

As explained on page 2 of the specification, conventional methods of parallel processing, such as demonstrated by the cited prior art Suetake, share a common memory area for the multiple processors, thereby making it difficult to guarantee that data or counting will not be contaminated during parallel or vector processing.

In contrast, by uniquely associating each additional processing unit with its own independently-functioning memory bank, the additional processing unit can lock-out access to its associated memory bank during the period it is processing its part of the operation, thereby safeguarding the information content without additional computer programming

techniques that are required when using a single memory area for all the processors (e.g., as used in Suetake). Moreover, as explained beginning at line 2 of page 25 and continuing through the final line on page 28, the associated memory banks of the present invention provides vectorization and/or parallelization capability beyond the conventional techniques described in these pages.

II. THE PRIOR ART REJECTIONS

The Examiner alleges that Suetake, when modified by either Roy or Sidman, renders obvious the present invention defined by claims 1-19.

Applicant again respectfully traverses that Suetake teaches or reasonably suggests the unique computer architecture defined by the independent claims or that modification by either Roy or Sidman would remedy the deficiency inherent in Suetake.

The Examiner continues to fail to heed the plain meaning of the claim language and seemingly fails to understand the significance of the feature of the present invention as having a memory bank uniquely associated with each additional processing unit.

As indicated in the previous Amendment, the memory banks of the present invention are not the internal registers 33, 34 of the processing units 30 shown in Figure 3. Rather, as shown in Figures 2 and 3, this claim language indicates the memory banks 40 external to the processing units 30 or main processor 11 (Figure 1) or 12 (Figure 2).

Although Applicant believes that one of ordinary skill in the art would understand this feature from the original claim wording, independent claims 1, 8, 13, and 14 have been amended above for clarity. Independent claim 19 requires no further clarification. None of the prior art currently of record demonstrates this unique feature of the present invention.

This feature allows each additional processing unit to lock out its associated memory bank during the time it is processing data, thereby providing a simple method of guaranteeing data and counting integrity for vectorization and parallelization.

For example, as explained in the first full paragraph on page 25 of the specification, the present invention addresses the problem in which an array "count" or two-dimensional array "list" can be incorrectly updated.

Suetake fails to incorporate this design approach of localized, automonous memory units for each slave processor. That is, as clearly shown in Figure 8, the slave processor 802

and CPU 801 share access to the main cache 805 and main memory unit 806.

In the rejection currently of record, the Examiner relies upon the architecture shown in Figure 10 as corresponding to the description of the independent claims. However, the processing pipelines and/or internal registers shown in Figure 10, upon which the Examiner seems to consider as equivalent to the "memory banks" of the claimed invention, are internal to the slave processor 802 and are somewhat analogous to the internal registers 33-38 of the additional processors 30, as shown in Figure 3 of the present disclosure.

Applicant submits that, to one of ordinary skill in the art, these operating registers, internal to a processing unit, are not equivalent to the term "memory bank", particularly given the clarification of the claim language in independent claims 1, 8, 13, and 14. Applicant again submits that one of ordinary skill in the art would consider this terminology as a term of art and that a "memory bank" is not at all equivalent to an internal operating register or an operational pipeline.

Although the Examiner is allowed to make a reasonably broad interpretation, that interpretation must be consistent with an interpretation that one of ordinary skill in the art would agree, as clearly stated in MPEP §2111: "*The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach.*"

For at least the reasons stated above, Applicant respectfully submits that Suetake fails to teach or suggest every feature of the independent claims and, indeed, clearly demonstrates exactly the problem being addressed by the present invention for parallel processing that uses a common memory area.

In paragraph 3 on page 2 of the Office Action, the Examiner alleges that Suetake "... did not expressly detail (claims 1, 8, 13, 14-19) that the memory banks corresponded to the processor units or locking out access to the memory banks."

Applicant respectfully traverses this characterization of Suetake, since Figure 9 clearly shows that register 910 are internal to the vector unit 901. Applicant submits that these register are irrelevant to the invention defined in the independent claims, since the present invention includes registers 32,34 internal to the additional processor units 30, as clearly shown in Figure 3.

Applicant submits that the relevant component in Suetake is main memory unit 806

shown in Figure 8, and this memory is clearly shared by the CPU 801 and slave processor 802. Therefore, Suetake clearly teaches against the concept of the present invention in which each additional processor unit has it own memory bank that it can isolate from other memory during processing.

The Examiner's initial burden, if Suetake is to be relied upon as the primary reference, is to justify a position that it would be obvious to modify Suetake by replacing main memory unit 806 with individual memory banks, one for each slave processor.

Since the rejection currently of record fails to allege such modification, Applicant submits that this rejection fails as a *prima facie* rejection under 35 USC §103(a).

Hence, turning to the clear language of the claims, in Suetake there is no teaching or suggestion of: "...additional processing units, each of which corresponds to one of the memory banks ... said plurality of memory banks being external to said processing unit and external to said additional processing units", as required by claim 1. The remaining independent claims have similar language.

Therefore, the Examiner is respectfully requested to withdraw these rejections based on Suetake.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Moreover, relative to the Examiner's motivation to combine either Roy or Sidman with Suetake, Applicant submits that "... reducing memory access latency" is already achieved in Suetake by use of the cache memory 805. That is, there would be no relative benefit of "reducing memory access latency" in Suetake by replacing main memory unit with separate memory bank units since each of these memory bank units would still be connected to the memory bus 808, 809 via the cache memory 805.

Finally, Applicant submits that, even if Suetake were to be modified by either Roy or Sidman, the modification would not overcome the basic deficiency identified above for Suetake wherein is explicitly taught to use a common main memory 806.

That is, not only does the primary reference Suetake teach against the modification required to satisfy the plain language of the independent claims, neither Roy nor Sidman teaches or suggests the feature of the present invention in which each additional processor unit corresponds to one of the memory banks external to the processor unit.

First, relative to Sidman, the register banks 100, 102 in Figure 3 of Sidman are internal to the processor 10.

Second, relative to Roy, the memory cluster concept taught therein may or may not be appropriate as implementing concepts of the present invention, since it is irrelevant that the present invention could be achieved by a combining existing references, as clearly stated in MPEP §2143.01: "*The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.*" As previously mentioned, the primary reference Suetake teaches a single memory 806, thereby teaching against the urged modification. Indeed, the switching capability 24_1-24_4 shown in Figure 1, wherein the inputs at ports 25c-25m are freely switched among the clusters 33, indicates that this reference also teaches using a common memory for all of the input ports.

Therefore, Applicant submits that Roy represents, at most, one possible component that might be utilized to realize the present invention but that neither Suetake nor Roy suggests using the capability of Roy in the environment of Suetake or to add the necessary additional control to ensure that the memory clusters of Roy would be locked out during processing by the slave processor 802 shown in Figure 8 of Suetake.

That is, Applicant submits that the Examiner's initial burden, if Suetake and Roy are to be used as prior art, would be to demonstrate that Roy provides a suggestion to dedicate one of the clusters uniquely to each slave processor 802, while allowing CPU 801 controlled access to that uniquely-assigned cluster. Applicant submits that the Examiner does not point out such suggestion in Roy.

Further, the other prior art of record has been reviewed, but it too even in combination with Suetake, Roy, or Sidman, fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-19, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance,

the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 3/22/05

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